

Claims

- 1 1. A method for forming a structure, the method comprising:
2 forming a layer over a substrate, the layer having a depletion region having a
3 thickness less than approximately 20 angstroms;
4 removing a portion of the layer to define a gate of a transistor, the gate defining a
5 channel length;
6 introducing a plurality of dopants into the substrate proximate the gate to define a
7 source and a drain; and
8 heating the substrate to a temperature to activate the plurality of dopants,
9 wherein the temperature is sufficiently low to prevent at least a portion of the
10 plurality of dopants from diffusing enough to induce a high off current.
- 1 2. The method of claim 1 wherein the substrate comprises an insulating
2 layer.
- 1 3. The method of claim 2 wherein the substrate comprises a strained layer
2 disposed over the insulating layer.
- 1 4. The method of claim 1 wherein the substrate comprises a strained layer.
- 1 5. The method of claim 4 wherein the strained layer is tensilely strained.
- 1 6. The method of claim 4 wherein the strained layer is compressively
2 strained.
- 1 7. The method of claim 1 wherein the substrate comprises a relaxed layer.
- 2 8. The method of claim 1 wherein the substrate comprises germanium.
- 1 9. The method of claim 1 wherein the induced off current is less than 10^{-6}
2 Amperes per micrometer.

1 10. The method of claim 9 wherein the induced off current is less than 10^{-9}
2 Amperes per micrometer.

1 11. The method of claim 1 wherein after the plurality of dopants are
2 introduced, a portion of the plurality of dopants disposed in a region of the source define
3 a source extent proximate the channel, and after heating the substrate, the source extent
4 diffuses under the gate a distance extending less than 12.5% of the channel length.

1 12. The method of claim 11 wherein a concentration of the portion of dopants
2 at the source extent is at least approximately 10^{18} atoms/cubic centimeter.

1 13. The method of claim 1 wherein after the plurality of dopants are
2 introduced, a portion of the plurality of dopants disposed in a region of the drain define a
3 drain extent proximate the channel, and after heating the substrate, the drain extent
4 diffuses under the gate a distance extending less than 12.5% of the channel length.

1 14. The method of claim 13 wherein a concentration of the portion of dopants
2 at the drain extent at least approximately 10^{18} atoms/cubic centimeter.

1 15. The method of claim 1 wherein the layer comprises a semiconductor and
2 the step of forming the layer includes introducing a plurality of gate dopants into the
3 layer, and heating the layer to a first temperature to alter a distribution of the gate dopants
4 in the layer.

1 16. The method of claim 15 wherein the semiconductor comprises silicon.

1 17. The method of claim 1 wherein the semiconductor comprises germanium.

1 18. The method of claim 1 wherein the layer comprises a metallic element.

1 19. The method of claim 18 wherein the metallic element comprises at least
2 one of molybdenum, titanium, tantalum, tungsten, iridium, nickel, cobalt, and platinum.

1 20. A method for forming a structure, the method comprising:

2 introducing a first plurality of dopants into a gate electrode layer disposed over a
3 substrate;

4 heating the gate electrode layer to a first temperature to alter a distribution of the
5 first plurality of dopants in the gate electrode layer;

6 removing a portion of the gate electrode layer to define a gate of a transistor;

7 introducing a second plurality of dopants into the substrate proximate the gate to
8 define a source and a drain; and

9 heating the substrate to a second temperature to activate the second plurality of
10 dopants,

11 wherein the second temperature is less than the first temperature.

1 21. The method of claim 20 wherein the substrate comprises an insulating
2 layer.

1 22. The method of claim 21 wherein the substrate comprises a strained layer
2 disposed over the insulating layer.

1 23. The method of claim 20 wherein the substrate comprises a strained layer.

1 24. The method of claim 23 wherein the strained layer is tensilely strained.

1 25. The method of claim 23 wherein the strained layer is compressively
2 strained.

1 26. The method of claim 20 wherein the substrate comprises a relaxed layer.

1 27. The method of claim 20 wherein the substrate comprises germanium.

1 28. The method of claim 20, wherein the first temperature is greater than 1000
2 °C.

1 29. The method of claim 20, wherein the second temperature is less than 1000
2 °C.

1 30. The method of claim 20 wherein the gate electrode layer comprises a
2 semiconductor layer.

1 31. The method of claim 30 wherein the semiconductor layer comprises
2 silicon.

1 32. The method of claim 30, wherein the semiconductor layer comprises
2 germanium.

1 33. The method of claim 20 wherein the first plurality and the second plurality
2 of dopants comprise n-type dopants.

1 34. The method of claim 20 wherein the first plurality and the second plurality
2 of dopants comprise p-type dopants.

1 35. A method for forming a structure, the method comprising:
2 introducing a first plurality of dopants into a gate electrode layer disposed over a
3 substrate;
4 heating the semiconductor layer for a first time period to alter a distribution of the
5 first plurality of dopants in the gate electrode layer;
6 removing a portion of the gate electrode layer to define a gate of a transistor;
7 introducing a second plurality of dopants into the substrate proximate the gate to
8 define a source and a drain; and
9 heating the substrate for a second time period to activate the second plurality of
10 dopants,
11 wherein the second time period has a shorter duration than a duration of the first
12 time period.

1 36. The method of claim 35 wherein the substrate comprises an insulating
2 layer.

1 37. The method of claim 36 wherein the substrate comprises a strained layer
2 disposed over the insulating layer.

- 1 38. The method of claim 35 wherein the substrate comprises a strained layer.
- 1 39. The method of claim 38 wherein the strained layer is tensilely strained.
- 1 40. The method of claim 38 wherein the strained layer is compressively
2 strained.
- 1 41. The method of claim 35 wherein the substrate comprises a relaxed layer.
- 1 42. The method of claim 35 wherein the substrate comprises at least one of
2 silicon and germanium.
- 1 43. The method of claim 35 wherein the first time period is greater than 5
2 seconds.
- 1 44. The method of claim 35 wherein the first time period is greater than 30
2 seconds.
- 1 45. The method of claim 35 wherein the gate electrode layer comprises a
2 semiconductor layer.
- 1 46. The method of claim 45 wherein the semiconductor layer comprises
2 silicon.
- 1 47. The method of claim 45 wherein the semiconductor layer comprises
2 germanium.
- 1 48. The method of claim 35 wherein the first and the second plurality of
2 dopants comprise n-type dopants.
- 1 49. The method of claim 35 wherein the first and the second plurality of
2 dopants comprise p-type dopants.
- 1 50. A structure comprising:
2 a strained layer disposed over a substrate, and
3 a first transistor including:

4 a first source and a first drain, wherein at least a portion of the first source
5 and a portion of the first drain are disposed in a first portion of the strained layer;
6 a first gate disposed above the strained layer and between the source and
7 drain, the first gate comprising a first metal; and
8 a first gate dielectric layer disposed between the first gate and the strained
9 layer.

1 51. The structure of claim 50 wherein the substrate comprises a dielectric
2 material and the strained layer is disposed in contact with the dielectric material.

1 52. The structure of claim 50 wherein the first metal is selected from the
2 group consisting of titanium, tungsten, molybdenum, tantalum, nickel, cobalt, and
3 platinum.

1 53. The structure of claim 50 wherein the strained layer comprises silicon.

1 54. The structure of claim 50 wherein the gate comprises a metal-
2 semiconductor alloy.

1 55. The structure of claim 54 wherein the gate consists essentially of the
2 metal-semiconductor alloy.

1 56. The structure of claim 50, further comprising:
2 a channel disposed under the gate.

1 57. The structure of claim 56 wherein the source comprises a source extent
2 proximate the channel, the source extent extending under the gate a distance less than
3 12.5% of a channel length.

1 58. The structure of claim 57 wherein a concentration of dopants in the source
2 extent is at least approximately 10^{18} atoms/cubic centimeter.

1 59. The structure of claim 56 wherein the drain comprises a drain extent
2 proximate the channel, the drain extent extending under the gate a distance less than
3 12.5% of a channel length.

1 60. The structure of claim 59 wherein a concentration of dopants in the drain
2 extent is at least approximately 10^{18} atoms/cubic centimeter.

1 61. The structure of claim 50, further comprising:

2 a second transistor including:

3 a second source and a second drain, wherein at least a portion of the
4 second source and a portion of the second drain are disposed in a second portion of the
5 strained layer;

6 a second gate disposed above the strained layer and between the second
7 source and second drain, the second gate comprising a second metal; and

8 a second gate dielectric layer disposed between the second gate and the
9 strained layer,

10 wherein the first transistor is an n-type metal-oxide semiconductor field-effect
11 transistor, the first source and the first drain comprise n-type dopants, the second
12 transistor is a p-type metal-oxide-semiconductor field-effect transistor, and the second
13 source and second drain comprise p-type dopants.

1 62. The structure of claim 61 wherein the first gate has a first workfunction,
2 the second gate has a second workfunction, and the first workfunction is substantially
3 equal to the second workfunction.

1 63. The structure of claim 61 wherein the first gate has a first workfunction,
2 the second gate has a second workfunction, and the first workfunction is substantially
3 different from the second workfunction.